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EXAMINER	
FAHERTY, COREY S	

ART UNIT	PAPER NUMBER
2183	

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12/17/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/611,377	LIPPINCOTT ET AL.	
	Examiner	Art Unit	
	Corey Faherty	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the reply filed on 10/01/2009.

2. Claims 1-9 and 11-29 are pending in the application and have been examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7, 9, 11-16 and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Gove (U.S. Patent 5,613,146).

5. Regarding claims 1 and 27, Gove discloses a data driven processing method, comprising: providing a first set of instructions and incoming data to a first processing unit, of a data driven processor, to operate upon said incoming data [col. 34, lines 61-67; data is operated on]; configuring a data path for transferring data between a second processing unit of the data driven processor and external memory [col. 13, lines 25-42; a transfer data path is configured]; and the first processing unit, in response to recognizing that the first set of instructions will require one of reading from and writing to external memory, provides addressing information to a memory access unit of the processor to enable the transfer of additional data between the external memory and the second processing unit via said data path [col. 13, lines 25-42; col. 58, lines 36-42; addressing information is provided for the transfer].

6. Regarding claim 2, Gove discloses the method of claim 1 wherein the first processing unit recognizes an image processing motion vector in said first set of instructions, and said additional data is to be written to the external memory and includes a macro block generated by the second processing unit based on the motion vector [col. 13, lines 25-42; col. 58, lines 20-29; col. 14, lines 55-58].

7. Regarding claim 3, Gove discloses the method of claim 1 wherein the data path is configured by an external host controller [Fig. 52 and accompanying description; OR col. 13, lines 25-42].

8. Regarding claim 4, Gove discloses the method of claim 1 further comprising: the first processing unit providing an indication to the memory access unit of whether the transfer is one of a read and a write [col. 58, lines 36-42].

9. Regarding claim 5, Gove discloses a data processor comprising: a first direct memory access (DMA) unit [col. 13, lines 1-10]; and a plurality of processing units each having a plurality of data ports, the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the DMA unit [col. 13, lines 25-42; col. 58, lines 16-29], the plurality of processing units are essentially identical units each having a plurality of sides, each side having a plurality of unidirectional data ports being an input port and an output port wherein the input port is programmable to route incoming data to any one of the output ports [col. 54, line 60 - col. 55, line 13], wherein one of the processing units has a control port from which it is to send information to the DMA unit about setting up a DMA channel through which one of data to be consumed and result data by one of the processing units is transferred [col. 13, lines 25-42].

10. Regarding claim 6, Gove discloses the processor of claim 5 further comprising: memory interface circuitry, wherein the DMA unit is to access external memory via the memory interface circuitry [col. 58, lines 20-29].

11. Regarding claim 7, Gove discloses the processor of claim 6 further comprising a host interface through which a host processor is to configure data flow between the data ports [Fig. 52 and accompanying description; OR col. 13, lines 25-42], wherein the memory interface circuitry is on-chip with the DMA unit, the plurality of processing units, and the host interface [abstract].

12. Regarding claim 9, Gove discloses the processor of claim 5 wherein each of the processing units has an input programming element (PE) to read incoming data from any one of its input ports [Fig. 30 and accompanying description], an output PE to write result data to any one of its output ports [Fig. 30 and accompanying description], and a core PE to execute instructions independently of a data path that is operating through a pair of the input and output ports of that processing unit [Fig. 30 and accompanying description].

13. Regarding claim 11, Gove discloses the processor of claim 6 wherein each of the plurality of processing units has a plurality of control ports on each side including an input control port and an output control port, and wherein the input control port of a processing unit is programmable to route incoming command information to any one of the output control ports of said processing unit [Fig. 30 and accompanying description].

14. Regarding claim 12, Gove discloses the processor of claim 9 further comprising an interface to an external device, and wherein the output ports of one of said processing units are coupled to the input ports of an adjacent one of said processing units except that some of the

output ports of an outlying one of said processing units are coupled to the external device interface [Fig. 17].

15. Regarding claim 13, Gove discloses the processor of claim 5 further comprising: a second DMA unit [Fig. 17, master processor], wherein there are at least four of said plurality of processing units, the data ports on a north side of first and second ones of said four processing units are coupled to the first DMA unit, the data ports on a south side of third and fourth ones of said four processing units are coupled to the second DMA unit, and the data ports of a south side of the first and second processing units are coupled to the data ports of a north side of the third and fourth processing units [Fig. 17].

16. Regarding claim 14, Gove discloses the processor of claim 13 further comprising an interface to an external device, wherein some of the data ports of east and west sides of the processing units are coupled to the external device interface [Fig. 17].

17. Regarding claim 15, Gove discloses the processor of claim 5 further comprising a central processing unit to read and execute instructions that configure the data ports and the DMA unit to create a data channel from one of the processing units to external memory [col. 13, lines 25-42].

18. Regarding claim 16, Gove discloses the processor of claim 5 further comprising a host interface unit to receive instructions, from an external host controller, that configure the data ports and the DMA unit to create a data path from one of the processing units to external memory [Fig. 52 and accompanying description; OR col. 13, lines 25-42].

19. Regarding claim 28, Gove discloses the processor of claim 27 further comprising means for ensuring that said lower level memory accesses meet signal level and timing requirements of external memory [Fig. 20 and accompanying description].

20. Regarding claim 29, Gove discloses the processor of claim 27 further comprising means for expanding the data processor [Fig. 4].

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

23. Claims 8 and 17-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove.

24. Regarding claim 8, Gove does not explicitly disclose that the external memory is dynamic random access memory. However, the benefits of DRAM are well known in the art (structural simplicity, high density) and its use as external memory in the system of Gove would therefore have been obvious.

25. Regarding claims 17 and 23, Gove discloses a system comprising: a host controller [Fig. 17]; external memory [Fig. 17]; a data driven processor having a memory access unit to interface the external memory [Fig. 17], a plurality of processing units each having a plurality of data ports [Fig. 17; Fig. 30], the data ports being coupled to each other and programmable to allow data flow from any one of the processing units to another and from any one of the processing units to the memory access unit [Fig. 17; Fig. 30; col. 58, lines 16-42], and a host interface unit to receive instructions from the external host controller that configure the data ports and the memory unit to create a data path from one of the processing units through a data channel to the external memory [col. 13, lines 25-42; col. 34, lines 61-67], wherein one of the processing units has a control port which it uses to write data location information to the memory access unit [col. 58, lines 36-42]. Gove does not explicitly disclose one of a rechargeable battery and a fuel cell coupled to power the external memory, the host controller, and the data driven processor. However, the benefits of using rechargeable battery technology (portability) are well known in the art and the use of such technology in the system of Gove would therefore have been obvious.

26. Regarding claim 18, Gove discloses the system of claim 17 wherein the host controller includes an embedded processor and its associated main memory [Fig. 17; Fig. 29].

27. Regarding claims 19 and 25, Gove does not explicitly disclose that the couple of each pair of data ports from adjacent processing units is a point-to-point unidirectional connection. However, the use and benefits of point-to-point connections in array processing systems are well known in the art and such use would therefore have been obvious in the system of Gove.

28. Regarding claim 20, Gove discloses the system of claim 19 wherein each of the processing units has a core programming element (PE) that can be programmed to execute

instructions that operate on incoming data received via an input data port of that processing unit [Fig. 30], an input PE that can read data from any one of a plurality of input data ports of that processing unit [Fig. 30; Fig. 17], and an output PE that can write data to any one of a plurality of output data ports of that processing unit [Fig. 30; Fig. 17].

29. Regarding claim 21, Gove discloses the system of claim 20 wherein the core PE of each processing unit can execute its instructions independently of a data path that is operating through a pair of said input and output data ports of that processing unit [Fig. 17, 29, 30 and accompanying descriptions].

30. Regarding claim 22, Gove discloses the system of claim 17 wherein the data location information that is sent through the control port includes information about the size and display location of a block of image data [col. 58, lines 36-42].

31. Regarding claims 24 and 26, Gove discloses the system of claim 23 wherein each of the processing units has a plurality of control ports that are connected to each other in a mesh arrangement [Fig. 17; Fig. 30] so that the data channel information, including one of a read and write command, address, and memory access unit channel identifier, can originate from any one of the processing units and be routed to the memory access unit via a logical control channel programmed in the mesh arrangement [col. 58, lines 16-42].

Response to Arguments

32. Applicant's arguments filed 10/01/2009 have been fully considered but they are not persuasive.

33. Applicant argues that the Gove reference does not teach a "data driven processor". Applicant's basis for this argument is that the system of Gove is a von Neumann architecture and therefore can not anticipate a "data driven processor" because the two types are mutually exclusive. The problem with this argument is that, while the concept of a "data driven processor" is well known, there is no single well-understood list of requirements that are needed for a system to be "data driven". On the contrary, the term can and does refer to many different and varying combinations of design techniques. As shown below, applicant's specification does not make it clear which of these design techniques are intended, and the examiner is therefore required to interpret the term such that any of those techniques anticipate the claims. One such technique that is common to "data driven" systems is that of processing data in response to it becoming available. Gove clearly discloses at least using this technique [col. 3, lines 8-20] and therefore anticipates a "data driven system". It should be noted that this is only one of a multitude of interpretations of Gove that can be used to anticipate the term in question.

Regarding the specification, applicant has cited paragraph 0002 as describing the differences between a von Neumann architecture and a data driven processor. The paragraph first describes a von Neumann architecture, stating: "The von Neumann type processor is controlled by a clocked addressing scheme that can pull instructions and data from almost anywhere in memory."

The paragraph next describes a data driven processor as a system "designed to be fed blocks of data that are typically consecutively stored in memory (or arrive as a stream) and are to be processed according to a program that has only a small number of instructions that operate on the data."

It is immediately apparent how useless these teachings are in helping the examiner determine the scope of the claim term “data driven processor”. The specification intentionally uses extremely broad terminology that is both non-binding ("typically") and vague ("a small number"). For the examiner to read such language into the claim would be inappropriate because there is no evidence that it is intended to define the term in question. Furthermore, even if the examiner did read this disclosure into the claim language, it is so broad and vague that the cited prior art would still be anticipatory.

Having determined that the specification is not helpful in determining the scope of the claim, the examiner is left to explore the term as it is understood in the art. As stated above, the term as it is used in the art refers to many different combinations of design techniques and is therefore very broad. Applicant's remarks submitted on 10/01/2009 include references to internet search results and documents that supposedly make clear the definition of the claim terminology. However, no such search results or documents have been received by the office. Furthermore, applicant has not indicated which aspects of the data driven systems described in those documents are to be used in defining the scope of the claimed term.

In summary, applicant’s position appears to be that the term "data driven processor" requires specific subject matter that is not disclosed by Gove. However, the examiner cannot simply guess at what that subject matter might be. If applicant wishes to overcome the present rejections, applicant must state what that specific subject matter is and either include it in the claim language or offer evidence from the specification and the art that such subject matter is well understood to be required by the term.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Corey Faherty whose telephone number is (571)270-1319. The examiner can normally be reached on weekdays between 7:00 and 4:30, with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J. Huisman/
Primary Examiner, Art Unit 2183

/Corey Faherty/
Examiner, Art Unit 2183